

REMARKS/ARGUMENTS

This Amendment is submitted in response to the Office Action dated June 13, 2007, and within the period for reply extending to September 13, 2007. The current status of the claims is summarized as follows:

5 Claims 23-24 are cancelled.

Claims 1-22 are pending in the application after entry of the present Amendment.

Specification

10 Paragraph [0001] of the specification has been amended to provide the application serial number of the cross-referenced U.S. patent application and delete the corresponding attorney docket number. Therefore, the Office is kindly requested to withdraw the objection to the specification.

Allowable Subject Matter

15 The Applicants acknowledge the Office's indication that claims 11-17 are allowed. The Applicants also acknowledge the Office's indication that claims 4, 6, and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

20 Additionally, the Applicants submit that the Office's position with regard to the allowability of claim 6 is unclear. As mentioned above, the Office has indicated that claim 6 is objected to. However, the Office has also indicated that claim 6 is rejected under 35 U.S.C. 102. The Office is requested to clarify the status of claim 6. Also, as discussed below, the Applicants submit that claim 6 is patentable for at least the same
25 reasons as claim 1 from which it depends.

Rejections under 35 U.S.C. 102

Claims 1-3, 6, 8-10, and 18-24 were rejected under 35 U.S.C. 102(e) as being anticipated by Measor (U.S. Patent Application Publication No. US 2001/0007577).

5 These rejections are traversed.

The Office has asserted that the serializer 300 of Measor (Figure 3) teaches each and every feature of the assembler of claim 1, as required for anticipation under 35 U.S.C. 102. The Applicants respectfully disagree.

10 Claim 1 recites an assembler of a bandwidth matching device that includes a plurality of inputs and a plurality of multiplexers being equal in number to the plurality of inputs. The serializer 300 of Measor (Figure 3) does not teach a plurality of multiplexers being equal in number to a plurality of inputs. Specifically, the Office has asserted that the TWENTY inputs D0 through D19 as depicted in the serializer 300 of Measor represents the plurality of inputs recited in claim 1. The Office has also asserted that the
15 FOUR selector trees 301a through 301d as depicted in the serializer 300 of Measor represents the plurality of multiplexers recited in claim 1. The Applicants submit that FOUR selector trees 301a through 301d is not equal in number to TWENTY inputs D0 through D19.

The Office has vaguely asserted that the twenty inputs D0 through D19 of Measor
20 can be separated into four distinct sets, and each distinct set of inputs can be considered to teach one of the plurality of inputs as recited in claim 1. In following the Office asserts that because the four selector trees 301a through 301d in the serializer 300 of Measor is equal in number to the four distinct sets of inputs, the serializer 300 of Measor teaches a plurality of multiplexers (selector trees) equal in number to a plurality of inputs (distinct
25 input sets). However, this assertion by the Office has no merit.

First, claim 1 does not recite a plurality of input sets. Claim 1 recites a plurality of inputs. Therefore, the Office's assertion that a distinct set of five of the twenty inputs D0 through D19 of Measor can be considered to represent one input of the plurality of inputs as recited in claim 1 is not credible. Measor does not teach that a set of five of the twenty
5 inputs D0 through D19 can be considered to represent a single input. Moreover, the Office has not cited anything in Measor that would support such an assertion. Additionally, Measor [0036] specifically teaches that "each of selector trees 301a-d is capable of receiving and muxing 5 data inputs." Measor [0036] further teaches that the data inputs are collectively labeled D0-D19. Measor [0036] also teaches that each of the
10 twenty data inputs D0 through D19 corresponds to a respective bit of a twenty-bit word to be received by the serializer 300 in a parallel manner. Therefore, it is not reasonable to interpret Measor as teaching that five separate ones of the inputs D0 through D19 can be considered to represent a single input.

Measor is clear in teaching that each of selector trees 301a-d receives five separate
15 inputs. Therefore, the FOUR selector trees 301a-d of Measor collectively receive TWENTY inputs D0 through D19. Consequently, the number of selector trees 301a-d of Measor (FOUR) does not equal the number of inputs D0-D19 of Measor (TWENTY). In view of the foregoing it should be understood that the serializer 300 of Measor does not teach a plurality of multiplexers equal in number to the plurality of inputs as recited in
20 claim 1.

Furthermore, claim 1 recites that each of the plurality of multiplexers is connected to receive the plurality of inputs. It should be appreciated that claim 1 does NOT recite that each of the plurality of multiplexers is connected to receive SOME of the plurality of inputs. Rather, claim 1 carefully recites that each of the plurality of multiplexers is
25 connected to receive THE plurality of inputs. Therefore, each of the multiplexers in the

assembly of claim 1 is recited to receive the plurality of inputs in total. In contrast, the serializer 300 of Measor teaches that each selector tree 301a-d receives a DIFFERENT PORTION of the number of inputs D0 through D19. Therefore, it should be appreciated that Measor does not teach that each of the selector trees 301a-301d receives the plurality of inputs D0 through D19. Therefore, the serializer 300 of Measor does not teach each of the plurality of multiplexers being connected to receive the plurality of inputs, as recited in claim 1.

Furthermore, claim 1 recites that the stepped arrangement of cells is defined to generate a concatenated output representing a concatenated version of one of the plurality of inputs on a cycle of a clock. The serializer 300 of Measor is defined to output a SINGLE BIT on A CYCLE of a clock. Simply stated, a single bit does not represent a concatenated version of one of the plurality of inputs D0 through D19. Therefore, the serializer 300 of Measor does not teach a stepped arrangement of cells defined to generate a CONCATENATED OUTPUT representing a concatenated version of ONE of the plurality of inputs on A CYCLE of a clock.

For at least the reason discussed above, the Applicants submit that Measor fails to teach each and every feature of claim 1, as required to anticipate claim 1 under 35 U.S.C. 102. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Additionally, "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Furthermore, for a claim to be anticipated under 35 U.S.C. 102, the elements in the prior art must be arranged as required by the claim. *In re*

Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). Therefore, the Office is kindly requested to withdraw the rejection of claim 1 under 35 U.S.C. 102.

The Office has asserted that the serializer 300 of Measor (Figure 3) teaches each and every feature of the method for operating a bandwidth matching device of claim 18,
5 as required for anticipation under 35 U.S.C. 102. The Applicants respectfully disagree.

Claim 18 recites an operation for outputting sequential portions of one of the number of inputs from the stepped arrangement of cells of the assembler to provide a concatenated output containing the sequential portion. As discussed above, the serializer 300 of Measor is defined to output a single bit on a cycle of a clock. The single bit output
10 by Measor does not teach outputting sequential portions of one of the number of inputs to provide a concatenated output containing the sequential portions, as recited in claim 18.

Notwithstanding the fact that the serializer 300 of Measor teaches outputting a single bit on a each cycle of the clock, Measor definitely does not teach outputting sequential portions of ONE of the number of input D0 through D19. Sequential portions
15 of ONE of the inputs D0 through D19 of Measor would correspond to sequential instances of a common bit (one of either D0 through D19). Measor clearly teaches away from outputting sequential instances of a common bit. Specifically, the serializer 300 of Measor realizes its functionality by outputting a different one of bit inputs D0 through D19 (i.e., a different one of the plurality of inputs) on successive clock cycles, thereby
20 serially outputting the bit inputs D0 through D19 having been previously received by the serializer 300 in a parallel manner.

For at least the reason discussed above, the Applicants submit that Measor fails to teach each and every feature of claim 18, as required to anticipate claim 1 under 35 U.S.C. 102. Therefore, the Office is kindly requested to withdraw the rejection of claim
25 18 under 35 U.S.C. 102.

The Office has asserted that the serializer 300 of Measor (Figure 3) teaches each and every feature of the device of claim 22, as required for anticipation under 35 U.S.C. 102. The Applicants respectfully disagree.

As with claim 1, claim 22 recites a plurality of inputs and a plurality of
5 multiplexers equal in number to the plurality of inputs. Also, as with claim 1, claim 22 recites that each multiplexer is coupled to receive the plurality of inputs. Furthermore, as with claim 1, claim 22 recites a plurality of cells to generate a cell output representing a concatenated version of a different one of the plurality of inputs in relation to a cycle of the clock signal. Therefore, the Applicants submit that the arguments presented above
10 with regard to claim 1 are equally applicable to claim 22. Thus, Measor does not teach each and every feature of claim 22 as required for anticipation under 35 U.S.C. 102. Therefore, the Office is kindly requested to withdraw the rejection of claim 22 under 35 U.S.C. 102.

Because a dependent claim incorporates each and every feature of the independent
15 claim from which it depends, the dependent claim is patentable for at least the same reasons as its independent claim. Therefore, the Applicants submit that each of dependent claims 2-10 and 19-21 is patentable for at least the same reasons as its respective independent claim.

The Office is requested to note that claims 23-24 are cancelled.

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In view of the foregoing, the Applicants submit that all of the pending claims are in condition for allowance. Therefore, a Notice of Allowance is requested. If the Examiner has any questions concerning the present Amendment, the Examiner is requested to contact the undersigned at (408) 774-6914. If any additional fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. SUNMP233). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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